design ideas

Edited by Bill Travis and Anne Watson Swager

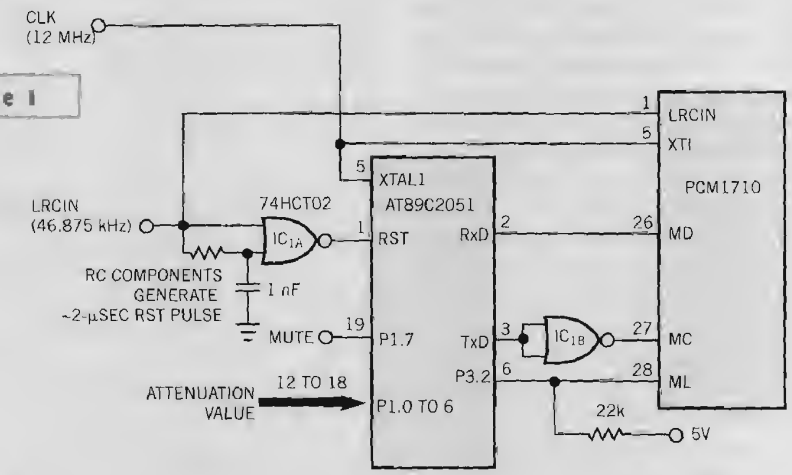
µC reprograms audio DAC via serial interface

Lukasz Sliwczynski, University of Mining and Metallurgy, Institute of Electronics, Cracow, Poland

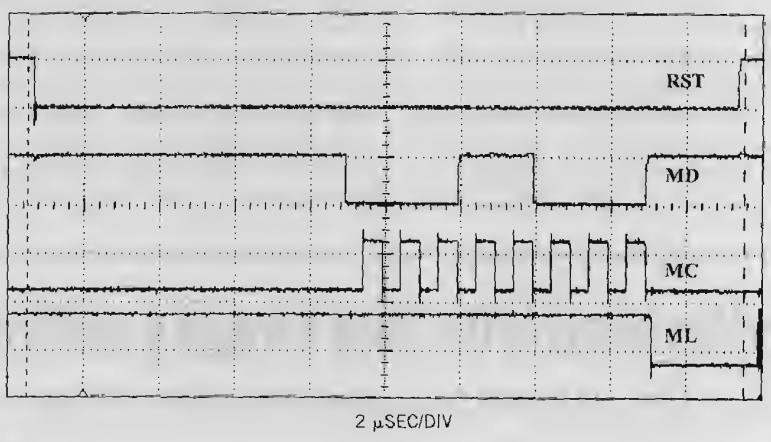
YOU CAN USE A SIMPLE µC to continuously program an audio DAC so that it operates in a 20-bit resolution mode (**Figure 1**). After power-on, the PCM1710 ΔΣ DAC (Burr-Brown Corp, www.burr-brown.com) operates in its default 16-bit resolution mode. Switching to its 20-bit resolution mode requires supplying the converter with a control word using its three-wire serial digital interface (SDI). A risk exists for using this converter at a resolution of 20 bits in a transmission system that should work 24 hours a day, seven days a week with no, or only occasional, supervision. A disturbance can cause reprogramming of the converter and cause it to revert to its default settings. The circuit in **Figure 1** eliminates this possibility by repeatedly reprogramming the DAC. The circuit uses the SDI to continuously supply three programming words, which define the converter's state of operation, to the DAC.

The reprogramming circuitry, which uses a popular AT89C2051 µC (Atmel, www.atmel.com), has few components and

Figure 1



(a)



(b)

A simple µC-based circuit (a) continuously reprograms the PCM1710 audio DAC for a resolution of 20 bits. The µC sends 1 byte of code after each RST pulse (b).

is power-efficient (**Figure 1a**). Because any µC system is also vulnerable to external disturbances, it's best to reset the µC repetitively. The circuit uses the LRCIN signal to reset the µC and invoke the programming procedure. The LRCIN signal also switches digital-audio words between the left and right channels of the converter. Thus, the µC takes less time to execute the program than the period of the LRCIN signal. The sampling rate is 46.875 kHz, so the period of the LRCIN signal is approximately 21 µsec. The circuit must devote some of this time to properly resetting the µC.

The SDI of the PCM1710 comprises data (MD), clock (MC), and latch (ML) lines. To drive this SDI, the serial port of the µC operates in the default mode, Mode 0. Although this mode of operation is rare in many applications, it is convenient in this case because, apart from sending serial data via its RxD pin (P3.0), the serial clock is available on the TxD pin (P3.1). Thus, the RxD line directly serves as the MD signal, and the inverted TxD line serves as the MC signal. The program generates the third SDI line (ML). Sending 3 bytes of data to the DAC requires at least 36 µsec, assuming a 12-MHz clock from the DAC clock and omitting the time that the internal reset procedure of the µC consumes. Thus, you can transmit 1 byte for one program execution, which occupies about 17 µsec. Assuming that 2 µsec is enough time for the µC to properly reset, the entire program should easily fit into the allowable 21-µsec frame. The low time of RST is approximately 19 µsec (**Figure 1b**).

This interface circuit relies on the fact that after you apply the RST signal to the µC, some internal registers do not change their values, and others reset to 00H. **Listing 1** is the corresponding assembler code. (You can download this listing from *EDN*'s web site, www.ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2312.) After each RST pulse, the µC sends 1 byte of code; the µC sends the same byte every third RST pulse. The circuit uses register R_0 to temporarily save the value of the next word to send because the µC reset does not affect this register. The circuit also uses one bit-addressable memory location, designated FLAG (20H), to switch between bytes to send. Port P1 supplies the program with the attenuation value on pins P1.0 to P1.6 (from MSB to LSB) and supplies the MUTE signal on pin P1.7. The circuit stores the proper value of the Mode 1 control word in the program-memory area of the µC at locations 60H (MUTE deasserted) and E0H (MUTE asserted). (DI #2312)

LISTING 1—PCM1710 DAC ASSEMBLER CODE

```
; ATTENUATION SET ON PORT P1.0 (MSB) - P1.6 (LSB)
.EQU PCON, 087H
.EQU FLAG.7, 07H
.EQU FLAG.6, 06H
.EQU FLAG.5, 05H


.ORG 00H
      JBC FLAG.7,B_03          ;2
      JBC FLAG.6,B_02          ;2 -> TOTAL MACHINE CYCLES: 4

B_01: MOV SBUF,R0              ;2 SEND ATTENUATION BYTE
      MOV R0,#25H              ;1 SAVE MODE 2 BYTE BEFORE RESET
      SETB FLAG.6              ;1 SET UP FOR THE NEXT RESET
      MOV A,#02H               ;1
      NOP                      ;1
      NOP                      ;1
      NOP                      ;1
      NOP                      ;1
      NOP                      ;1
      CLR P3.2                 ;1 GENERATE ML SIGNAL
      ORL PCON,A               ;1 GO TO POWER DOWN -> TOTAL MACHINE CYCLES: 12

B_02: MOV SBUF,R0              ;2 SEND BYTE MODE 2
      MOV A,P1                 ;1 READ MUTE SIGNAL FROM P1.7
      ANL A,#080H              ;1
      ORL A,#060H              ;1
      MOVC A,@A+DPTR           ;2 CALCULATE ADDRESS OF MODE 1 BYTE
      MOV R0,A                 ;1 SAVE MODE 1 BYTE BEFORE RESET
      SETB FLAG.7              ;1 SET UP FOR THE NEXT RESET
      MOV A,#02H               ;1
      CLR P3.2                 ;1 GENERATE ML SIGNAL
      ORL PCON,A               ;1 GO TO POWER DOWN

B_03: MOV SBUF,R0              ;2 SEND BYTE MODE 1
      MOV A,P1                 ;1 READ ATTENUATION FROM PORT P1.0 - P1.6
      RL A                     ;1
      ANL A,#0FEH              ;1
      MOV R0,A                 ;1 SAVE ATTENUATION VALUE BEFORE RESET
      SETB FLAG.5              ;1 SET UP FOR THE NEXT RESET
      MOV A,#02H               ;1
      NOP                      ;1
      NOP                      ;1
      CLR P3.2                 ;1 GENERATE ML SIGNAL
      ORL PCON,A               ;1 GO TO POWER DOWN

;MODE 1 BYTE FOR MUTE-OFF -> P1.7 = L
.ORG 060H
      .DB 001H

;MODE 1 BYTE FOR MUTE-OFF -> P1.7 = H
.ORG 0E0H
      .DB 041H
```

To Vote For This Design, Circle No. 427

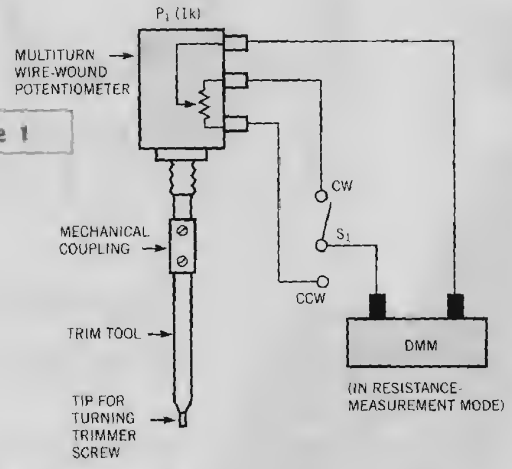
Calibrated trim tool tweaks multiturn pots

Sanjay Chendvankar, Tata Institute, Mumbai, India

Many analog circuits contain multiturn trimming potentiometers whose settings you may need to change during maintenance or calibration. Also, some instruments have panel-mounted potentiometers that may need periodic adjustments. After disturbing a setting by more than one or two turns, it becomes difficult or impossible to restore the original setting. The usual method is to measure the resistance between the wiper and one of the ends of the potentiometer before disturbing the setting and then to readjust to the same setting if and when necessary. However, this method is incon-

venient and sometimes impossible, such as when the trimmer is mounted on a panel, for example. The simple tool in **Figure 1** comes in handy in such situations.

Figure 1



This "tool with a memory" allows you to accurately restore the original setting of a multiturn potentiometer.

You construct the tool by mechanically coupling the trimming tool's shaft to the shaft of a high-quality, multiturn, wirewound potentiometer (P_1). The wiper and one of the end terminals of this potentiometer connect to a DMM operating in resistance-measurement mode. The toggle switch, S_1, selects one of the two available end terminals. Before disturbing the setting of a multiturn potentiometer in a circuit, you rotate the trim tool to the endpoint of P_1's rotation span in the opposite direction to that in which you intend to adjust the trimming potentiometer. Set the selector switch such that the DMM reads zero (or near-zero) resistance. Then, you rotate the trim tool by firmly holding P_1 with one hand and turn the trimming potentiometer to the desired setting. The corresponding P_1 resistance value on the DMM, along with S_1's position, tells you whether the tool rotates clockwise or counterclockwise. You record these data for future reference.

If you wish to restore the potentiometer's original position, you adjust P_1 to the recorded value with the same position of S_1 by turning the trim tool in the opposite direction until the DMM reads zero resistance. This position is the original setting of the potentiometer. The resistance value of P_1 is not critical. However, it's better to select low values to obtain higher resolution on the DMM. Also, a single range of the DMM should cover the value. This prototype uses 1 kΩ. You can improve the tool by replacing P_1 with a miniature bidirectional optical shaft encoder and connecting its output to an up/down counter. (DI #2308)

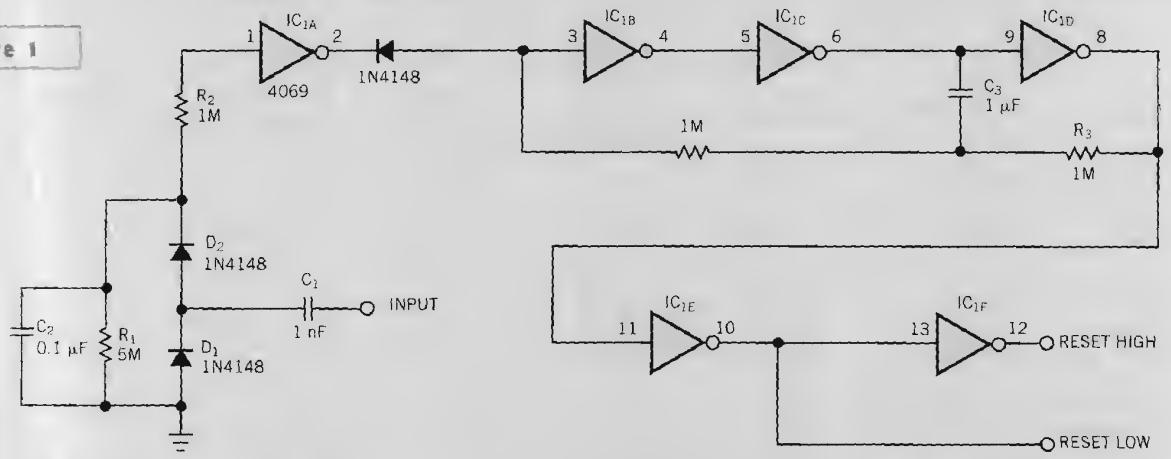
Off-the-shelf watchdog serves in a pinch

Giovanni Romeo, Istituto Nazionale di Geofisica, Roma, Italy

The performance of the watchdog circuit in **Figure 1** may not match that of a dedicated watchdog circuit, but this circuit is helpful when the only watchdog in the lab doesn't meet your design's temperature requirement and when you are in a hurry to finish a prototype.

The circuit operates on a simple principle. When digital activity occurs on the in-

Figure 1



A charge pump comprising D_1, D_2, C_1, and C_2 inhibits a three-gate oscillator when input activity exists. After 40 msec without input activity, the oscillator starts running and produces a reset signal.

put, a charge pump comprising C_1, D_1, D_2, and C_2 keeps C_2 charged. R_1 is the discharge resistor for C_2. IC_{1A} detects the charge level through R_2. A charged condition inhibits the three-gate oscillator comprising IC_{1B}, IC_{1C}, and IC_{1D}, and the active-high reset-high output stays low.

When the voltage at the input of IC_{1A} drops below the CMOS threshold, the oscillator starts working and produces a square wave. The high time of the reset-high output resets the µP under control, which must start the activity (and activate the watchdog input) before the end of the low time. R_3 and C_3 essentially control the high and low times, which have almost the same value.

Although this design monitors an RS-232C line, you can use the circuit to monitor a digital level. When monitoring an RS-232C line with the values in **Figure 1**, the watchdog starts resetting 40 msec after detecting no activity and requires less than 20 msec to inhibit the oscillator after input activity resumes. (DI #2311)

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Novel circuit controls ac power

Narendra Paranjape, Tata Chemicals Ltd, Mithapur, India

The simple and inexpensive power-control circuit in **Figure 1** uses a readily available fan regulator with built-in phase control. Such fan regulators are limited to approximately 100W. The circuit in **Figure 1** adds two SCRs and a few components to turn the humble fan regulator into a mighty power controller. The fan regulator operates with a nominal load of 10 to 25W through a lamp, which also gives a power-level indication. The 1:1:1 pulse transformer completes the circuit. The transformer's secondary windings fire the back-to-back SCRs, which then control a load of 1000 to 3000W. You can house the circuit in any insulated box. You should mount the SCRs on heat sinks. R_1, D_1 and R_2, D_2 limit the gate current and prevent the application of reverse voltage between gate and cathode. **Figure 2** shows construction details of the prototype. (DI #2310)

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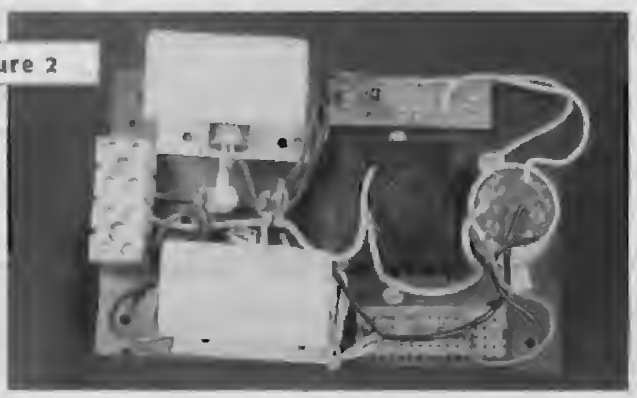
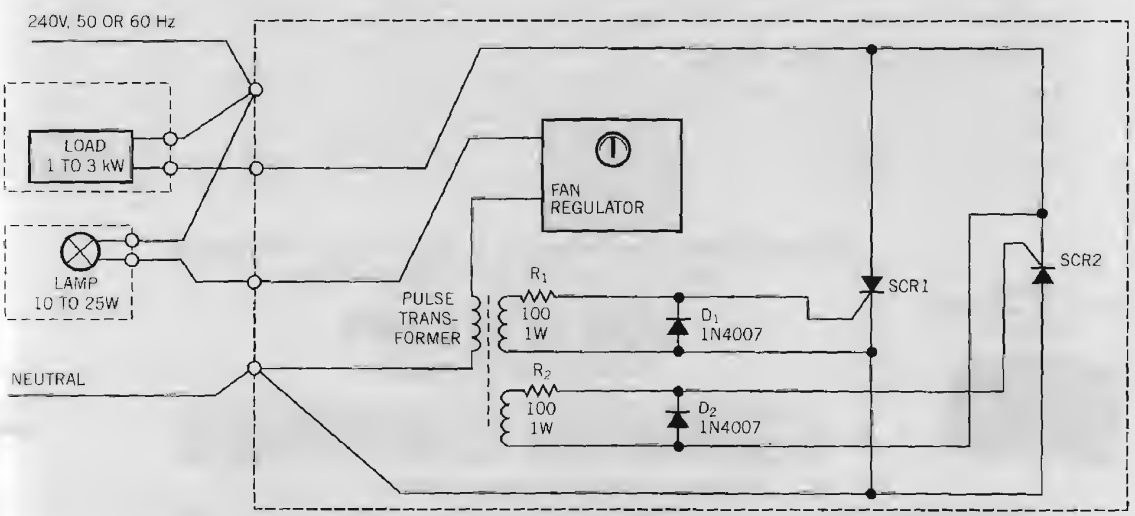
Figure 2



An easy-to-build power controller works with an inexpensive fan regulator to control 1000 to 3000W.

Figure 1



A couple of thyristors, a pulse transformer, and two diodes transform a humble 100W fan regulator into a high-power ac controller.

Two AA cells power step-down regulator

Len Sherman, Maxim Integrated Products, Sunnyvale, CA

DC/DC conversion is particularly challenging when both the input and output voltages are low. Step-up ICs that operate with inputs lower than 1V are available, but step-down ICs that accept input voltages near 2V are not. Thus, providing efficient power for the low-voltage CPU in a handheld product can be a problem if the power source is a two-cell AA battery. The battery's output can drop to 1.8V as the battery discharges. In **Figure 1**, the upper switch-mode dc/dc converter (IC_1) generates more than 600 mA at 1.5V, from a two-AA-cell input that varies from 3.4 to 1.8V. The 3.3V rail that powers this step-down controller comes from a high-current, synchronous-rectified boost controller (IC_3), which also provides power for external logic and the CPU's I/O blocks. IC_1 receives 3.3V bias, but power for the 1.5V output comes directly from the battery.

Q_2, D_2, and a SOT-23 reset IC (IC_2) force the switching power MOSFET (Q_1) off when the 3.3V rail is too low to properly operate IC_1. Without those components, the conditions at power-up (during which battery voltage is present but 3.3V are momentarily absent, pulling Q_1's gate low) may cause the 1.5V output to overshoot to the battery voltage. The 1.5V output's buck-conversion efficiency (approximately 85%) is reasonably good for the circuit's extra-small components: a three-pin SOT-23 power MOSFET and 5-mm-diameter surface-mount inductors. For the 3.3V output, IC_3's on-chip synchronous rectification yields a boost efficiency higher than 90%. (DI #2302)

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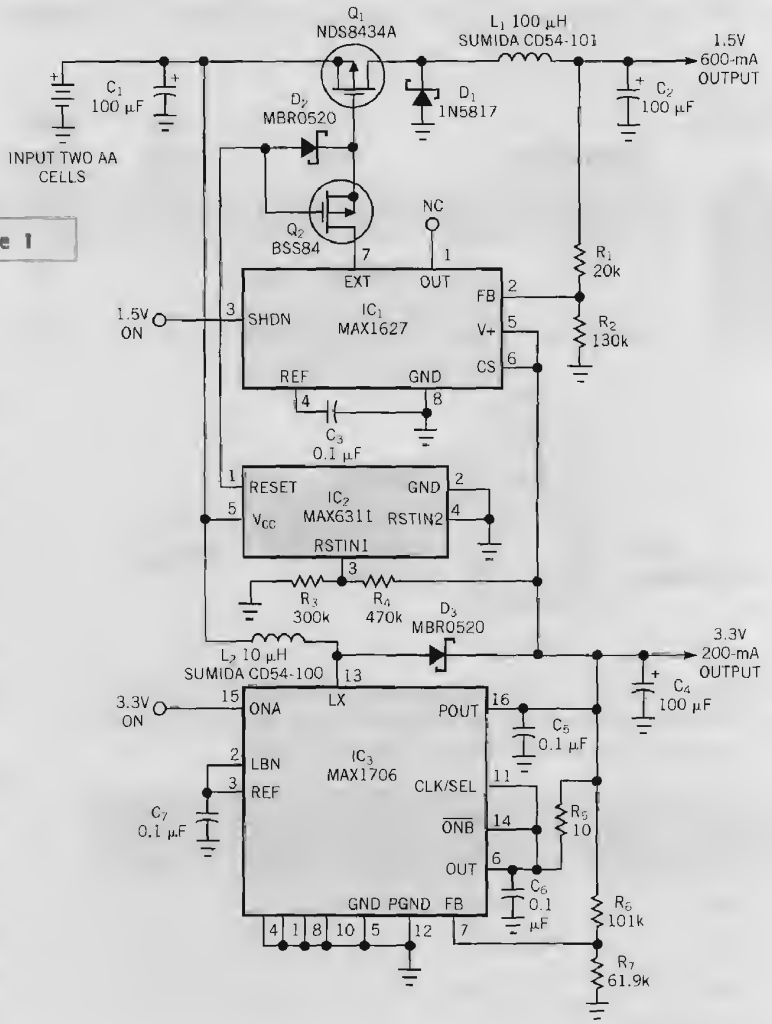
Figure 1



Powered by the 3.3V boost controller IC_3, this step-down controller (IC_1) generates 1.5V from inputs as low as 1.8V.

Temperature controller keeps IR detector at 8°K

Jerry Penegor, Space Sciences Laboratory, University of California—Berkeley

Sensitive infrared array detectors must operate at a low temperature to avoid thermally generated dark current throughout the photoconductive elements. This requirement is particularly true for SiAs array detectors, which need cooling to near liquid-helium temperatures. Furthermore, the sensitivity of these detectors can be temperature-dependent. The optimal operating temperature for a long-wavelength IR camera is about 8°K. This temperature must remain constant despite changes in the radiation level falling on the array, in the liquid helium level as it boils away, and

in the orientation of the Dewar flask.

To measure and control these low temperatures, the circuit in **Figure 1** uses a four-wire silicon diode. One pair of #38 AWG wire forward-biases the diode with a fixed 10 μA of drive current. The second pair of wires provides for Kelvin-connection measurement of the forward-voltage drop, V_F, which is a very nonlinear function of temperature. Around 8°K, the V_F is 1.5V and changes about –35 mV/°K. To accurately measure the array temperature requires mounting the diode as close as possible to the SiAs array in its ceramic chip carrier.

The back of this carrier is spring-loaded against an oxygen-free, high-conductivity copper plug onto which a 500Ω wirewound resistor attaches. A heavy copper braid also connects the plug to the liquid-helium reservoir. Good thermal contact between the power resistor and the chip carrier ensures that a simple circuit can control the temperature. The simple proportional-integral servo circuit in **Figure 1** can control array temperature to ±5 m°K over an 8 to 12°K range. Slewing the array to a new setpoint temperature takes approximately 30 sec.

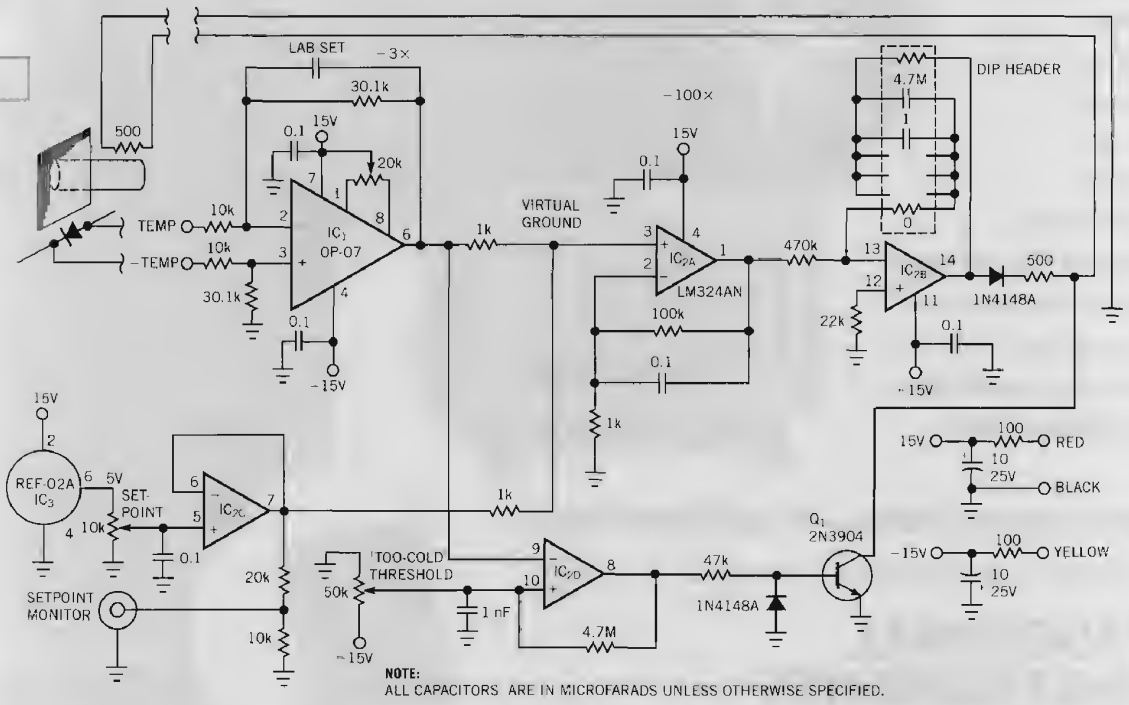
Special low-thermal-conductivity steel coax cable goes through hermetic connectors in the vacuum Dewar flask wall. This cable makes all electrical connections to the cooled camera. The schematic shows no low-leakage unity-gain buffers that isolate the voltages at the sensor diode's anode and cathode (+ and –T) from all the meters and circuitry that operate at room temperature.

Op amp IC_1 is a differential receiver for the + and –T voltages and has a gain of –3. Because –3 times the coldest expected V_F is about –4.8V, a stable 5V reference, IC_3, supplies the voltage at the potentiometer for the temperature setpoint over the necessary range. The setpoint-monitor output has an attenuation of 3, so you can see the setpoint voltage directly on any meter.

When the sensor and setpoint voltages are in balance, the noninverting input to IC_{2A} is 0V. IC_{2A} amplifies any imbalance. IC_{2B} sets the frequency response of the servo with a zero at a corresponding time constant of 10 sec. That is, IC_{2B}'s gain term of 10 is constant for any ac disturbances but is high for dc error. Mounting the resistors and capacitors that set the servo time constant on a seven-position header allows you to easily add component values when the controller is mounted on the Dewar flask. The output diode ensures that positive-only current goes to the power resistor on the heat sink; power off is 0V, and no negative currents can flow. (Negative current does not cool the power resistor.) The optional 500Ω series resistor in series with the output diode provides additional current limiting for IC_{2B}.

One condition to guard against is a broken or disconnected sense diode that sends the temperature controller into full-power application. IC_{2D} senses temperatures that are too cold—excessive negative voltage from IC—to be valid. The 50-kΩ potentiometer sets the "too-cold" threshold at approximately –5V. If the circuit detects a too-cold condition, IC_{2D} turns on Q_1, which shorts the output and sinks the output current within Q_1. (DI #2296)

Figure 1



NOTE:
ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

A four-wire silicon diode helps to maintain an IR camera's temperature at approximately 8°K. One pair of #38 AWG wires forward-biases the diode with a fixed 10 mA of drive current. A second pair of wires provides for a Kelvin-connection measurement of the diode's forward voltage drop, which is a nonlinear function of temperature.

Flyback circuit provides isolated power conversion

Philip Cooke, Unitrode Corp, Merrimack, NH

A COMMON REQUIREMENT in telecommunications systems is to convert an unregulated 48V line to an isolated, accurate dc supply voltage. The circuit in **Figure 1** provides a 5V, 15W output. The circuit uses a UCC3809 primary-side controller, which can also control other single-ended converters. The topology uses peak-current-mode control with a fixed-frequency oscillator. The design is cost-efficient, because it assumes that compensation of the voltage loop occurs on the secondary side, where you would place the error amplifier and reference anyway. By eliminating a primary-side amplifier, you reduce system cost and complexity.

The feedback signal from the secondary comes from the UC3965 precision reference. In addition to a low-offset error amplifier, this IC also contains an optocoupler driver for simplicity in designing isolated converters. An undervoltage-lockout circuit provides a controlled start-up transient. The design in **Figure 1** uses discontinuous-conduction mode (in which the flyback transformer undergoes complete demagnetization in every cycle), with maximum duty cycle set to 50%. Continuous-mode flyback circuits (in which the flyback transformer operates in continuous inductor-current mode) have a right-half-plane zero that limits the control bandwidth, as opposed to discontinuous-mode flybacks that do not restrict bandwidth.

Both ICs operate in either mode; the choice of mode depends on the power-supply requirements. You can easily buffer the primary-side oscillator with an emitter follower to provide slope compensation for designs requiring duty cycles beyond 50%. Note, however, that you have the option of programming a duty-cycle clamp to 50% or less, which can save cost by eliminating several slope-compensation components. The maximum-duty-cycle clamp in the UCC3809 is completely programmable by selecting the two resistors connected to pins 3 and 4. (DI #2288)

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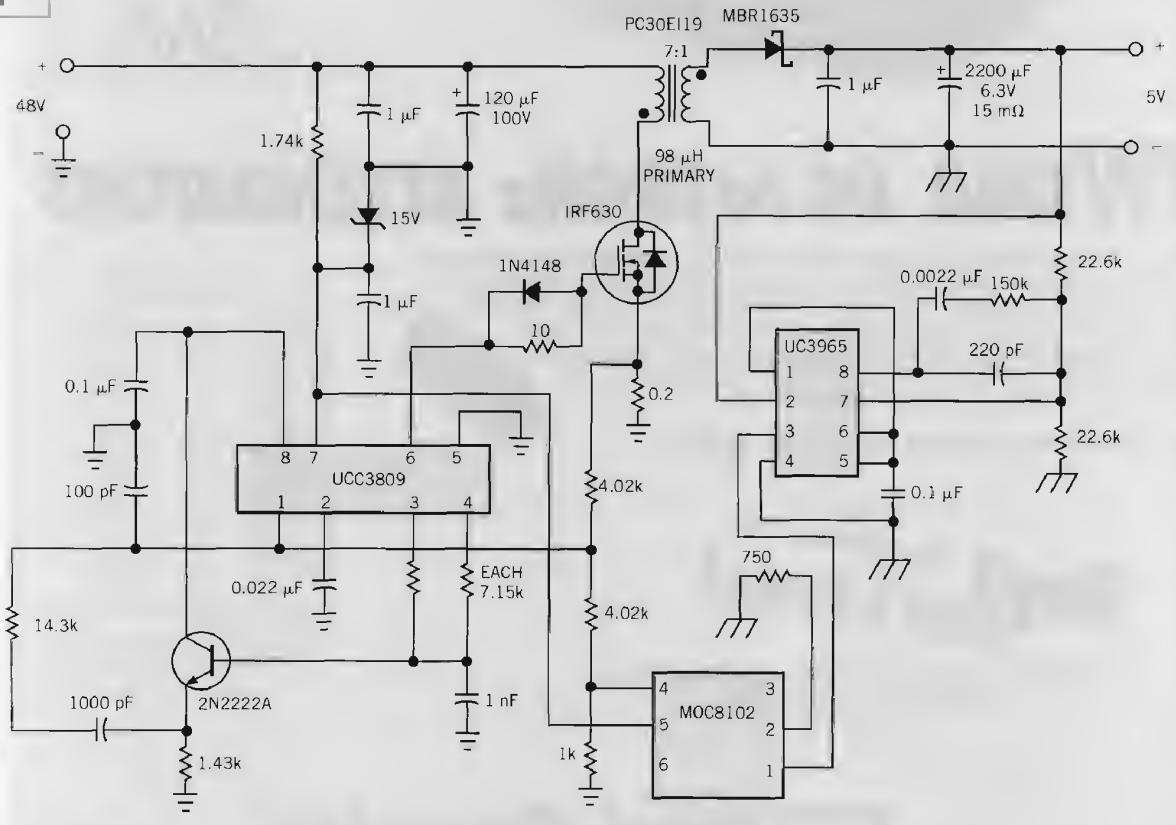
Figure 1



A discontinuous-mode flyback regulator provides an isolated, regulated supply, and saves cost by cutting compensation components.